Novel Design for Small-Size Coplanar Waveguide Frequency Tripler

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***Abstract*—This letter presents a novel design for a small-size coplanar waveguide frequency tripler. In this study, a new BPF has been replaced the conventional stub lines in the output termination of the multiplier. Not only enhance the performance of the tripler, but also reduce the whole circuit size. to 2.125×2.275 cm^2 in the frequency 0.8/2.4 GHz, The spurious suppressions are 37.48, 33.38, and 32.08 dBc for the 1st, 2nd, and 4th harmonics, respectively. It reveals the best output power of -1.92 dBm for a 0 dBm input signal and maximum conversion gain of -1.92 dB. It is very useful for applications in the wireless communication and radar systems.**

***Index Terms*—CPW structure, frequency multiplier, small-size BPF.**

I. Introduction

THE basic problem in designing a multiplier is achieving sufficient suppression of undesired signals at the output port. A balance topology offers the potential of superior even-harmonic suppression, and normal isolation [1]. But due to implementation of larger sized components such as couplers, a balanced design occupies too much area. In comparison to balanced topology, as reported in [2], single-ended CPW triplers have the capability of compact size. However, such design would require reflectors at both the input and output port to cancel the undesired harmonic signals. In general, several stub lines need to implement reflectors in triplers. Though, if one of the reflectors fails, the performance of the triplers would be degraded. The above problems may be improved by substituting it with a small size BPF [3]. But the conventional BPF such as parallel-coupled BPF, end-coupled . . . etc., still occupies too much area. It is to our knowledge that due to the conventional large-sized distributive BPF designs at less than 10 GHz, only few frequency triplers of such implementation have been discussed. Fabrication of such design is costly and becomes impractical on larger scale monolithic integration. Size reduction of the passive sections in MMIC is then an essential topic that shall not be neglected, which to us implies the necessity in better BPF design. Though recently there are some methods proposed to reduce size of filters [4], but it still occupies too much area. In this letter, a novel tripler with this topology is proposed as shown in Fig. 1. Using a compact-size CPW BPF [5], as a reflectors to suppress the undesired harmonics in this tripler. It would be discussed in detail in the Section II. This novel tripler provides a conversion gain of -1.92 dB for a 0 dBm input signal with a small circuit size of 2.125×2.275 cm^2. This circuit achieves high spurious suppressions above 30 dBc. It is quite useful for MICs and MMICs applications.

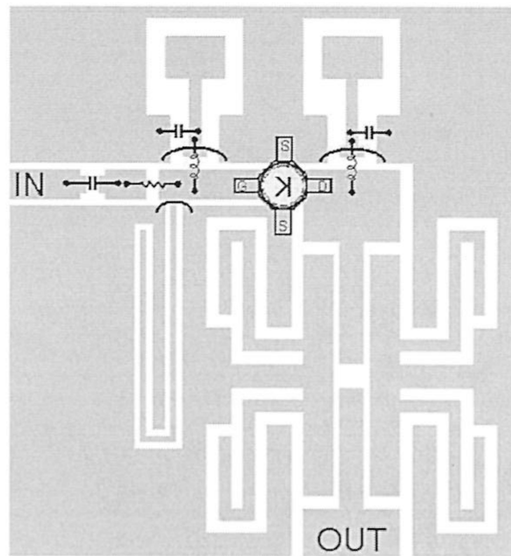

Fig. 1. Microwave frequency tripler with small-size CPW BPF.

II. Design Consideration

At the input port of the device, the $\lambda/4$ open-circuited stub is considered as RF short of the third harmonic power to enhance the conversion gain [6]. In conventional design, both shunt stub with capacitor and open stub are utilized as the output termination of the single-ended frequency multiplier in the MMIC design [2]. To improve the isolation of the circuit, one put the structure of parallel-coupled lines after the stub lines [7]. As well known by every designer, the best method about spurious suppression in single-ended mixer or multiplier is connecting with a BPF of sharp transition band at the output port for omitting all unwanted output harmonic powers which are produced by the active device due to the effect of nonlinearity. It means the conversion gain can be improved further. Unfortunately, not too many papers proposed with this idea because of the convectional BPF must be cascaded multistage to make the transition band sharp. It is the reason why the stub lines are still considered in the single-ended topology of frequency multiplier. Therefore, the compact sized BPF with sharp transition band will be suitable to utilize as the reflectors for suppressing the unwanted output signals.

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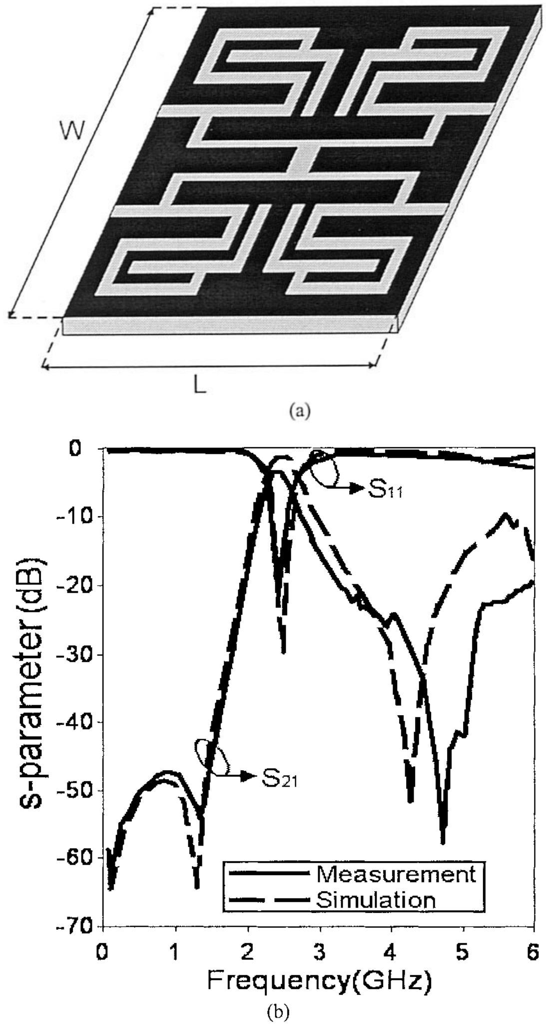

Fig. 2. Small-size CPW bandpass filter. (a) Circuit structure (W = 14 mm, L = 15 mm) and (b) performance.

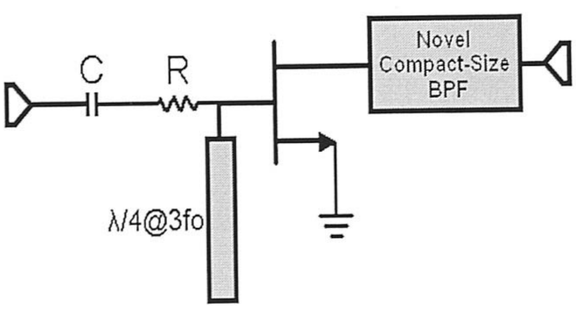

Fig. 3. Schematic diagram of the 0.8/2.4 GHz tripler. (R = 1 Ω and C = 1.8 pF).

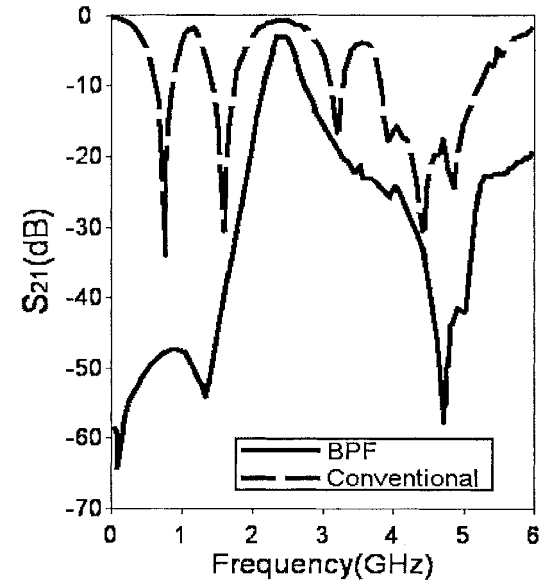

Fig. 4. Comparison of output termination of the tripler.

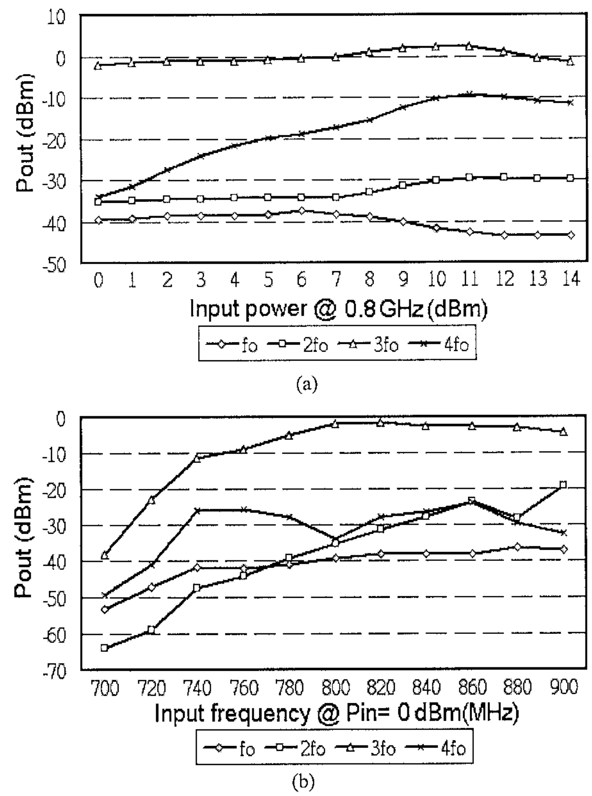

Fig. 5. Measured performance of the 0.8/2.4 GHz tripler. (a) Input power as function of the output power and (b) input frequency as function of the output power.

The conventional design of the output termination for the single-ended frequency multiplier needs to put the several stub lines after the active device. In this study, if one uses the conventional method to suppress unwanted harmonic signal by a shunt stub with capacitor to RF short the 0.8 GHz harmonic, and two shunt stubs to RF short the 1.6 GHz and 3.2 GHz harmonics, separately. The other way considers a novel BPF, which is shown in Fig. 2, to replace the conventional stub lines. The whole schematic diagram of this kind tripler is shown in Fig. 3.

The measured results for both cases are shown and compared in Fig. 4. It reveals that the spurious attenuations are more than 47, 38, and 19 dB for the first, second, and fourth harmonics, respectively. Obviously, the performance of the BPF is better than that of the conventional one; the block of the output termination in the tripler will be reduced by about 49%. The topology reveals an efficient way in size reduction and efficiency of the circuit design.

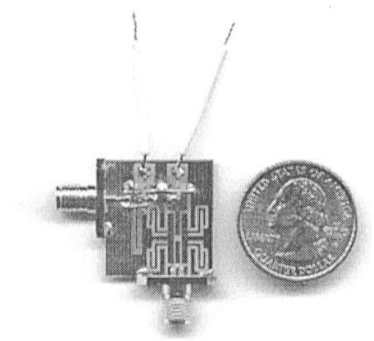

Fig. 6. Photograph of microwave CPW frequency tripler. (2.125×2.275 cm^2).

III. Implementation Results

All the implementation of circuits in this letter is fabricated on the FR4 substrate ($\varepsilon_r = 4.7, \tan\delta = 0.022, \mathrm{thickness} = 0.8\ \mathrm{mm}, \mathrm{metal\ thickness} = 0.02$ mm). The active device in the circuit is NEC NE3210S01, which is a pseudomorphic Hetero-Junction FET. The different operating classes of the transistor have been reported for MESFET-based frequency multiplier, such as the bias points close to class A, the odd harmonic power can be excited [8]. Fig. 5 shows the measured performance of the 0.8/2.4 GHz tripler. The measurement was done for a drain bias supply of 2 V and gate bias supply of -0.15 V, which corresponds to the class A condition. The circuit achieves best output power of -1.92 dBm for a 0 dBm input signal and a maximum conversion gain of -1.92 dB. The spurious suppressions are 37.48, 33.38, and 32.08 dBc for the first, second, fourth harmonics, respectively. Fig. 5(b) shows the well flatness of the input frequency from 800 to 900 MHz. The photograph of the fabricated MIC is shown in Fig. 6. The use of a single-ended topology with novel BPF technology results in a small circuit size of 2.125×2.275 cm^2. This same idea also applies for a 14.4/43.2 GHz tripler MMICs designs with very small circuit dimension (1 mm^2), and achieves high spurious suppression about 53.18 and 31.28 dBc for the 1st and 2nd harmonics, respectively.

IV. Conclusion

A novel CPW BPF successfully replaced the conventional stub lines as a reflector in the output termination of a 0.8/2.4-GHz tripler. It provides a conversion gain of -1.92 dB for a 0 dBm input signal with a small circuit size of 2.125×2.275 cm^2. This circuit achieves high spurious suppressions above 30 dBc. It is suitable to realize cost-efficient frequency sources and quite useful for MICs and MMICs applications.

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